WHAT IS CLAIMED IS:

1. A data communications adapter apparatus for coupling a host computer to a computer network employing communications media, the adapter comprising:

a) a transceiver coupled to receive and transmit data over the media;

b) a transmit data buffer;

c) data transmit control circuitry coupled to said transceiver, to said transmit data buffer, and to said host computer, for generating a packet transmit signal causing said transceiver to begin transmitting data from said transmit data buffer over said communications media;

d) a receive data buffer; and

e) data receive control circuitry coupled to said transceiver, to said receive data buffer, and to said host computer, for storing data received by said transceiver in said receive data buffer, and for generating a receive interrupt signalling to said host computer that data has been received by said transceiver, wherein said data receive control circuitry is operative to generate a receive interrupt once said transceiver has received over said communications media a predetermined number of bytes of a data packet less than all of said data packet.

2. The adapter of claim 1, further comprising:

a) ethernet control circuitry; and

b) host interface circuitry, wherein

said ethernet control circuitry, said host interface circuitry, said data receive control circuitry, said data transmit control circuitry, said receive data buffer and said transmit data buffer are all contained in a single Application Specific Integrated Circuit (ASIC).

3. The adapter of claim 1, wherein said data receive control circuitry is programmable.

4. The adapter of claim 1, wherein said data transmit control circuitry is programmable to generate said packet transmit signal when said transmit data buffer contains a predetermined number of bytes of a data packet less than all of said data packet.

5. A method of transferring a packet of data from a computer network communications media through an adapter to a host computer, said method comprising the steps of:

a) receiving from said communications media through a transceiver and storing in an adapter receive buffer a predetermined first receive threshold number of bytes of said packet;

b) thereupon generating a first early receive interrupt from said adapter to said host computer; and

c) thereafter receiving from said communications media through said transceiver and storing in said adapter receive buffer a remainder of said packet.

6. The method of claim 5, wherein said host computer employs a driver allowing for early indications and having an early lookahead size, and wherein step of receiving a predetermined first receive threshold number of bytes comprises receiving a number of bytes substantially equal to said early lookahead size.

7. The method of claim 5, wherein said host computer employs a driver allowing for early indications and having an early lookahead size, wherein said adapter and said host computer together have an interrupt latency time, said method further comprising after said step of receiving a predetermined first receive threshold number of bytes, the step of continuing to receive from said communications media through said transceiver and store in an adapter receive buffer bytes of said packet, wherein said step of receiving a predetermined first receive threshold number of bytes comprises receiving a predetermined first receive threshold number of bytes substantially equal to said early lookahead size less a

predetermined data receive rate times said interrupt latency time.

8. The method of claim 7, further comprising, after the step of generating said first interrupt, the steps of

a) evaluating the number of bytes stored in said adapter receive buffer against said early lookahead size; and

b) adjusting said receive threshold if said evaluating step does not indicate substantial equality.

9. The method of claim 5, wherein said packet comprises a preamble specifying a length of said packet in bytes, said method further comprising after said step of generating a first early receive interrupt and before said step of receiving a remainder of said packet, the steps of:

a) adjusting said receive threshold according to said length of said packet;

b) continuing to receive from said communications media through said transceiver and store in an adapter receive buffer bytes of said packet; and

c) thereafter generating a second early receive interrupt from said adapter to said host computer, prior to complete reception of said packet.

10. The method of claim 5, wherein said adapter receive buffer has a predetermined size, said method further comprising the steps of:

a) if additional bytes of a data packet are received from said communications media through said transceiver and stored in said adapter receive buffer while said adapter receive buffer contains allotted bytes of at least one packet not yet completely transferred to said host computer, such that the total number of allotted bytes in said adapter receive buffer is equal to said size of said adapter receive buffer less a predetermined adapter receive buffer free byte threshold, initiating a direct memory access (DMA) mode; and

b) receiving from said communications media through said transceiver and storing in a host computer receive buffer through DMA additional bytes of data.

11. A method of transferring a packet of data from a host computer through an adapter to a computer network communications media, said method comprising the steps of:

a) transferring from said host computer and storing in an adapter transmit buffer an early transmit threshold number of bytes of said packet;

b) thereupon initiating transmission of said packet through said transceiver from said adapter transmit buffer to said computer network communications media; and

c) receiving from said host computer and storing in said adapter receive buffer a remainder of said packet, at least partially in parallel with transmitting said packet through said transceiver from said adapter transmit buffer to said computer network communications media.

12. A method of transferring through an adapter packets of data between a host computer and a computer network communications media, said method comprising the steps of:

a) receiving from said communications media through said transceiver and storing in an adapter receive buffer a predetermined first receive threshold number of bytes of a first packet;

b) thereupon generating a first early receive interrupt from said adapter to said host computer;

c) receiving from said communications media through said transceiver and storing in said adapter receive buffer a remainder of said first packet;

d) transferring from said host computer and storing in an adapter transmit buffer an early transmit threshold number of bytes of a second packet;

e) thereupon initiating transmission of said second packet through said transceiver from said adapter transmit buffer to said computer network communications media;

f) receiving from said host computer and storing in said adapter receive buffer a remainder of said second packet, at least partially in parallel with transmitting said second packet through said transceiver from said adapter transmit buffer to said computer network communications media.

13. The method of claim 12, wherein each packet comprises a preamble specifying a length of said each packet in bytes, said method further comprising after said step of generating a first early receive interrupt and before said step of receiving a remainder of said first packet, the steps of:

a) adjusting said receive threshold according to said length of said first packet;

b) continuing to receive from said communications media through said transceiver and store in an adapter receive buffer bytes of said first packet; and

c) generating a second early receive interrupt from said adapter to said host computer prior to complete reception of said first packet.

14. The method of claim 13, wherein said adapter receive buffer has a predetermined size, said method further comprising the steps of:

a) if additional bytes of a data packet are received from said communications media through said transceiver and stored in said adapter receive buffer while said adapter receive buffer contains allotted bytes of at least one packet not yet completely transferred to said host computer, such that the total number of allotted bytes in said adapter receive buffer is equal to said size of said adapter receive buffer less a predetermined adapter receive buffer free byte threshold, initiating a direct memory access (DMA) mode; and

b) receiving additional bytes of data from said communications media through said transceiver and storing through DMA said additional bytes in a host computer receive buffer.

15. An electronic register stack structure for providing, for each of a plurality of actions, a condition represented by a predetermined number of condition flags, wherein said actions may have, upon completion, one of a first condition and at least one alternate condition, wherein a condition of one action at a time is currently accessible from said register stack structure, wherein the currently accessible condition may be removed from said register stack structure so as to make accessible a condition of a remaining action by popping said register stack structure, wherein storing conditions of said actions is halted upon an action having one of said at least one alternate condition, said register stack structure comprising:

a) a condition register comprising said predetermined number of condition flags;

b) a counter register;

c) means for storing a condition for a new action to said register stack structure by modifying contents of said condition register as necessary to indicate said condition of said new action and incrementing said counter register, wherein said counter indicates whether said currently accessible condition is to be said condition of said new action or a condition of a remaining action;

d) means for providing said currently accessible condition by

i) if said counter indicates that said currently accessible condition is to be said condition of said new action, providing contents of said condition register, and

ii) if said counter indicates that said currently accessible condition is to be a condition of a remaining action, providing said first condition; and

e) means for popping said register stack structure by decrementing said counter.

16. The register stack structure of claim 15, wherein said first condition is a successful condition and each said at least one alternate condition is an error condition.

17. The register stack structure of claim 15, wherein said means for providing said currently accessible condition further provides a zero condition when said counter indicates that all action conditions have been popped from said register stack structure.

add B1)